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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,452	01/15/2004	Satoshi Inoue	040840.01	4090

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EXAMINER	
PRENTY, MARK V	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,452	INOUE ET AL.	
	Examiner	Art Unit	
	MARK V PRENTY	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-7* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

This Office Action is in response to the RCE filed on September 20, 2004.

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claim 4 is indefinite because "the extension of the at least one end of the gate electrode" lacks antecedent basis in amended claim 3. Claim 4 should be amended to depend on independent claim 2 and to replace the above quoted language with "one of said extensions of the gate electrode."

Claims 1, 2 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherne et al. (United States Statutory Invention Registration H1435 - hereafter Cherne – cited in the Information Disclosure Statement filed on January 15, 2004) together with Hisamoto et al. (United States Patent 5,115,289 - hereafter Hisamoto – cited in the Information Disclosure Statement filed on January 15, 2004).

With respect to independent claim 1, Cherne discloses a thin film transistor including a plurality of component parts (see the entire reference, including the Figs. 11-12 disclosure), comprising: a channel region; a gate electrode opposed to the channel region; a gate insulating film provided between the channel region and the gate electrode; a source-drain region connected to said channel region; a source-drain wiring layer electrically connected to said source-drain region; and an extension of the gate electrode extending outwardly above and outside of the channel region (at least in the channel length direction between the source and drain).

The difference between claim 1 and Cherne is claim 1 also comprises a gate wiring layer electrically connected to the gate electrode (Cherne does not explicitly disclose a gate wiring layer electrically connected to its gate electrode).

Hisamoto teaches that a transistor's gate electrode is conventionally electrically connected to a gate wiring layer (see Hisamoto's Fig. 18a disclosure, for example, and note contact hole 510).

It would have been obvious to one skilled in this art to provide Cherne's transistor with a gate wiring layer electrically connected to the gate electrode, because Hisamoto teaches that a transistor's gate electrode is conventionally electrically connected to a gate wiring layer.

Claim 1 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Cherne together with Hisamoto.

With respect to independent claim 2, Cherne discloses a thin film transistor including a plurality of component parts (see the entire reference, including the Fig. 12 disclosure), comprising: a channel region; a gate electrode opposed to the channel region; a gate insulating film provided between the channel region and the gate electrode; a source-drain region connected to said channel region; a source-drain wiring layer electrically connected to said source-drain region; and extensions extending from both ends of the gate electrode outside of the channel region (at least in the channel length direction between the source and drain) and along a channel longitudinal [length] direction.

The difference between claim 2 and Cherne is claim 2 also comprises a gate wiring layer electrically connected to the gate electrode (Cherne does not explicitly disclose a gate wiring layer electrically connected to its gate electrode).

Hisamoto teaches that a transistor's gate electrode is conventionally electrically connected to a gate wiring layer (see Hisamoto's Fig. 18a disclosure, for example, and note contact hole 510).

It would have been obvious to one skilled in this art to provide Cherne's transistor with a gate wiring layer electrically connected to the gate electrode, because Hisamoto teaches that a transistor's gate electrode is conventionally electrically connected to a gate wiring layer.

Claim 2 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Cherne together with Hisamoto.

With respect to dependent claim 5, Cherne teaches that thin film transistors are used in CMOS architectures (see the Background of the Invention) and Hisamoto teaches that an inverter circuit is one such CMOS architecture (see Hisamoto's Figs. 18a-18b disclosure).

It would have been obvious to one skilled in this art to use the obvious Cherne/Hisamoto thin film transistors in a CMOS inverter circuit because Cherne teaches that thin film transistors are used in CMOS architectures and Hisamoto teaches that an inverter circuit is one such CMOS architecture.

Claim 5 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Cherne together with Hisamoto.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cherne et al. (United States Statutory Invention Registration H1435 - hereafter Cherne – cited in the Information Disclosure Statement filed on January 15, 2004) together with Hisamoto et al. (United States Patent 5,115,289 - hereafter Hisamoto – cited in the Information Disclosure Statement filed on January 15, 2004) and Yamazaki et al. (United States Patent 5,959,313 – hereafter Yamazaki – cited in the Information Disclosure Statement filed on January 15, 2004).

Claims 6 and 7 depend on independent claim 1. The explanation of the above rejection of independent claim 1 under 35 U.S.C. 103(a) as being unpatentable over Cherne together with Hisamoto is hereby incorporated by reference into this rejection of dependent claims 6 and 7 under 35 U.S.C. 103(a) as being unpatentable over Cherne together with Hisamoto and Yamazaki.

The difference, therefore, between claims 6 and 7 and the obvious Cherne/Hisamoto device is claim 6 recites a display device comprising a driving circuit including a thin film transistor according to claim 1 and claim 7 recites an electronic apparatus comprising a display device as defined in claim 6.

Yamazaki teaches using thin film transistors in a display device's driving circuit and using that display device in an electronic apparatus (see Yamazaki's Fig. 6 disclosure).

It would have been further obvious to one skilled in this art to use the obvious Cherne/Hisamoto thin film transistor in a display device's driving circuit and to use that display device in an electronic apparatus, because Yamazaki teaches using thin film transistors in a display device's driving circuit and using that display device in an electronic apparatus.

Claims 6 and 7 are thus rejected under 35 U.S.C. 103(a) as being unpatentable over Cherne together with Hisamoto and Yamazaki.

Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest the allowable thin film transistor taken as a whole, including the gate electrode extension.

The applicant's arguments with respect to the maintained rejections based on Cherne are not persuasive. Specifically, the applicant's allegation: "Cherne discloses in Figures 11 and 12 that the gate structure is positioned directly above the body/channel region. Thus, no part of the gate structure extends outside of the body/channel region," is without merit, because although Cherne's (Prior Art) Figures 11 and 12 are unclear as to whether their gate electrodes extend outside of their body/channel regions in the channel width direction (i.e., in the page's horizontal direction), their gate electrodes clearly do extend outside of their body/channel regions in the channel length direction (i.e., in the vertical direction from the source to the drain).

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

Mark Prenty

Mark V. Prenty
Primary Examiner